

FIG. 1

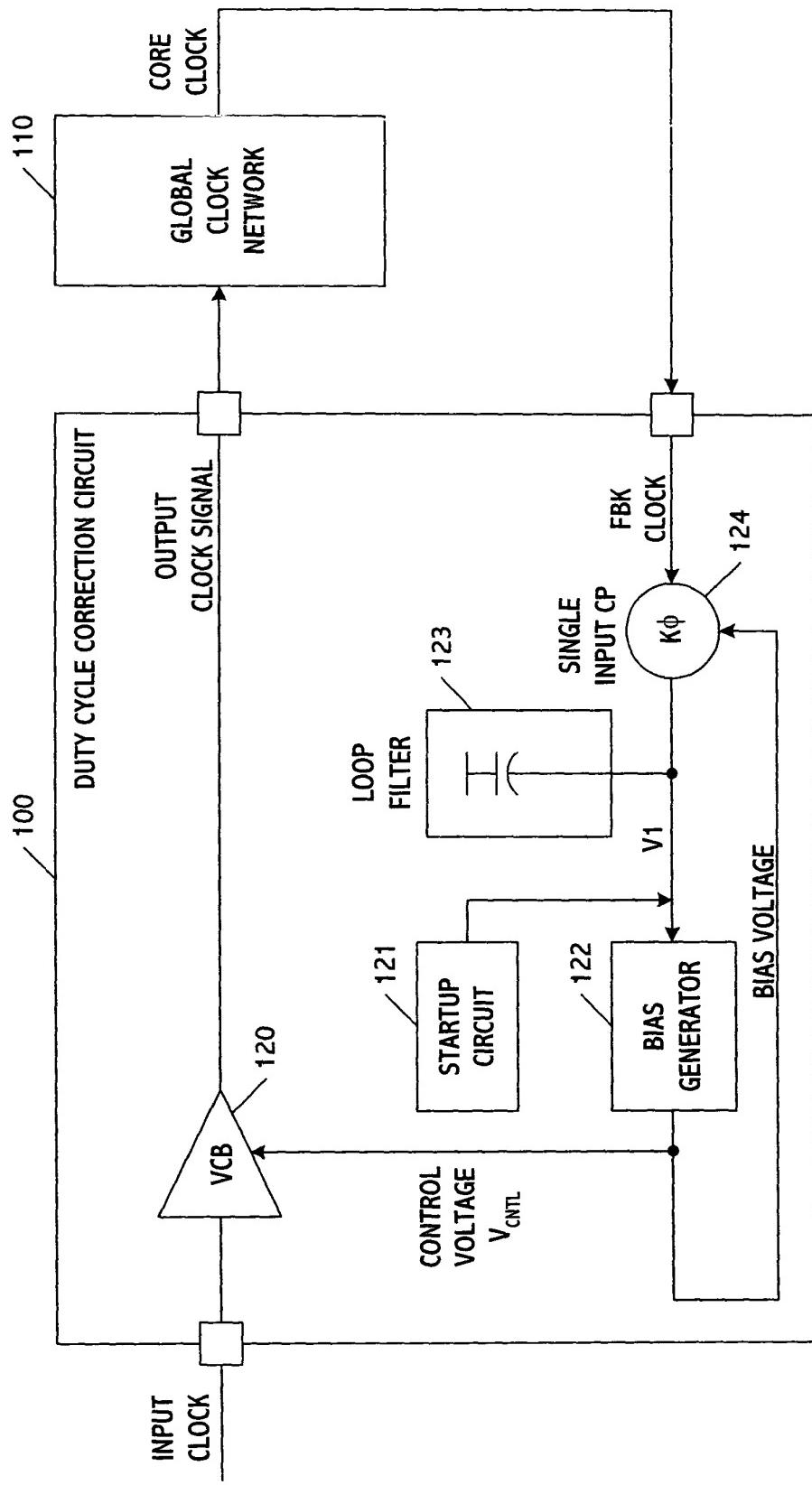


FIG. 2

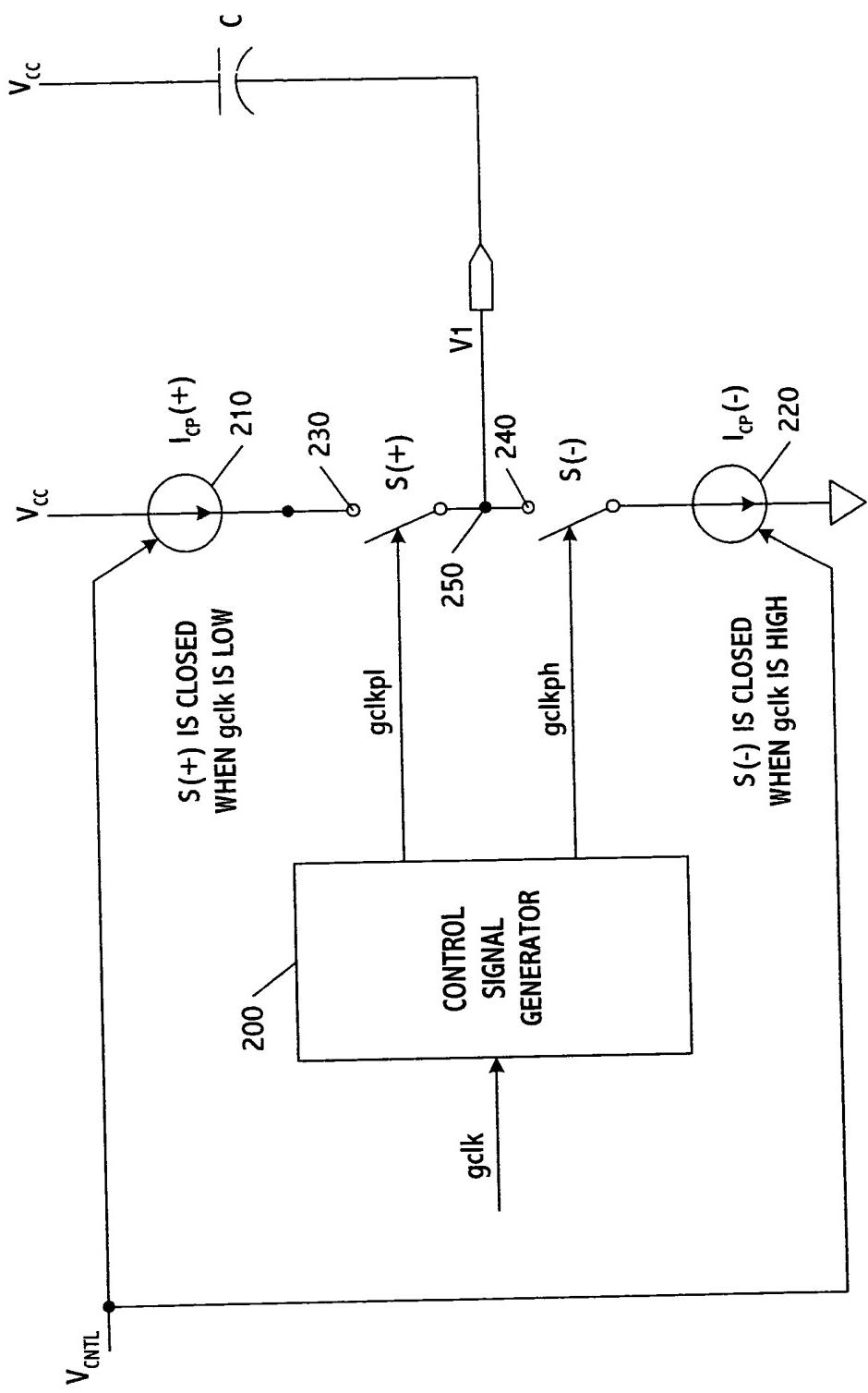


FIG. 3(a)

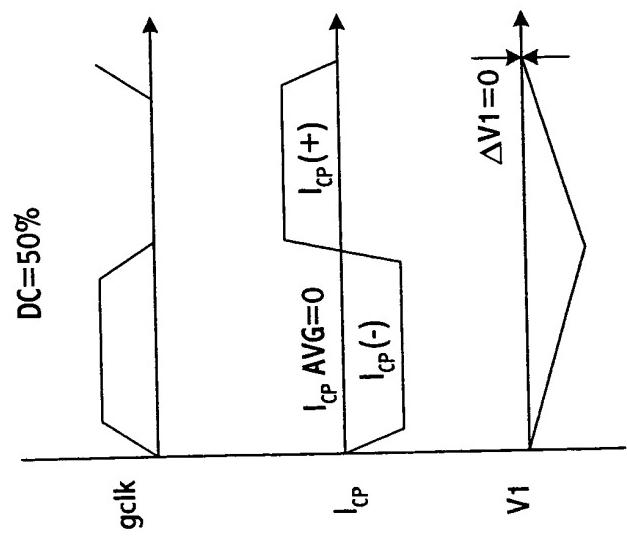


FIG. 3(b)

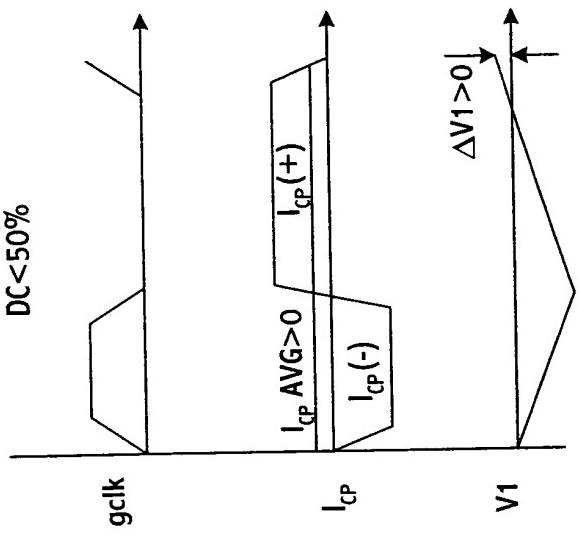


FIG. 3(c)

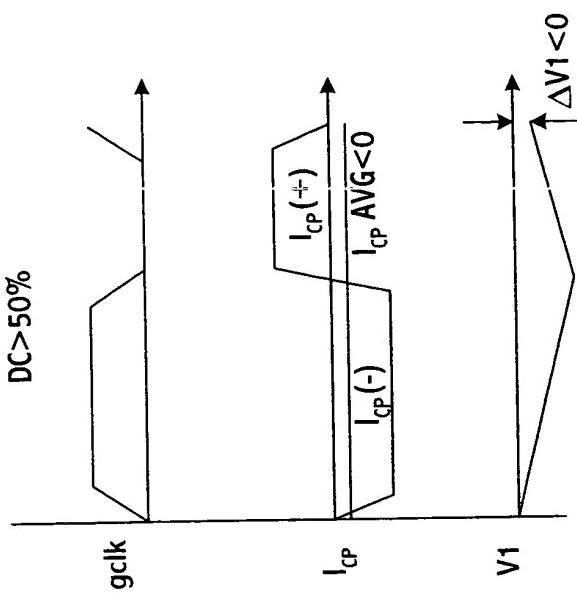


FIG. 4

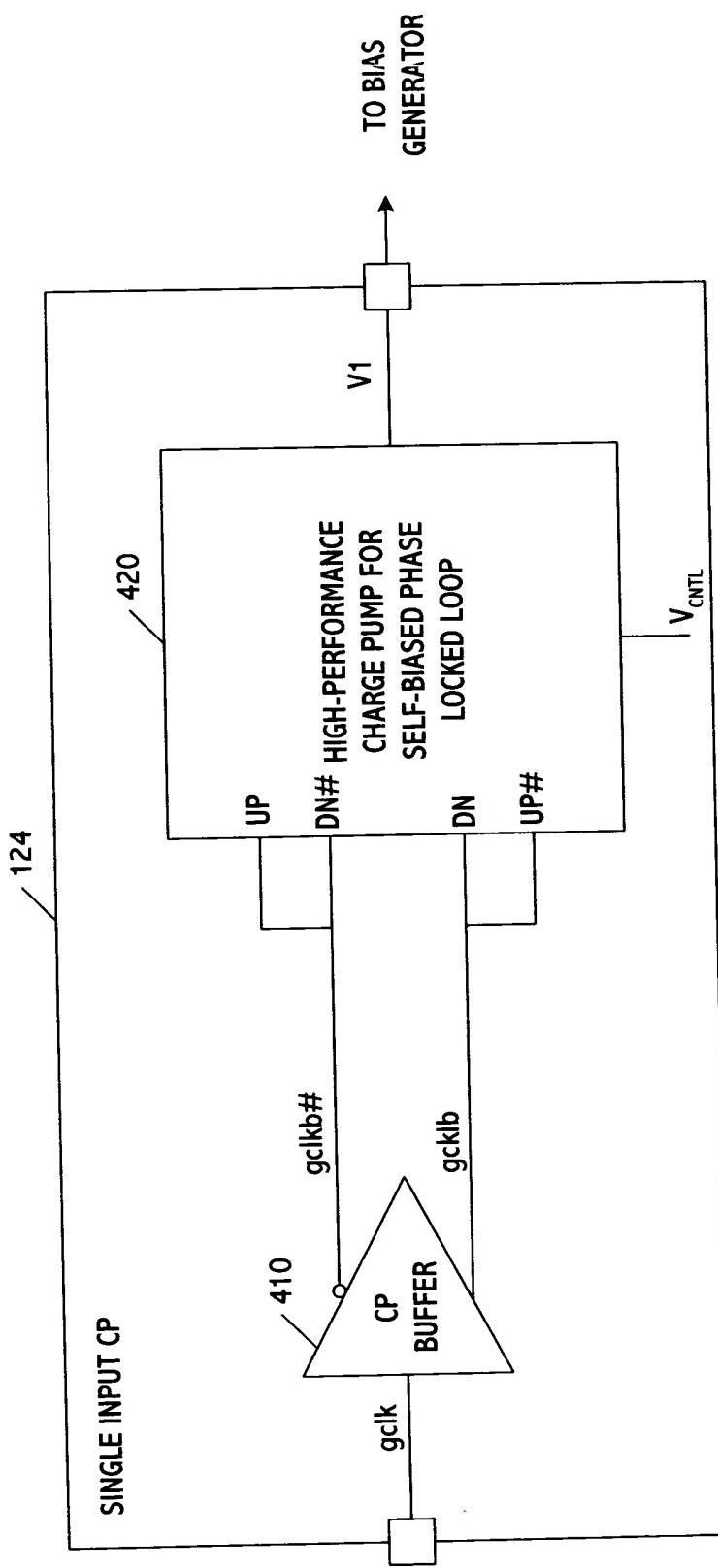
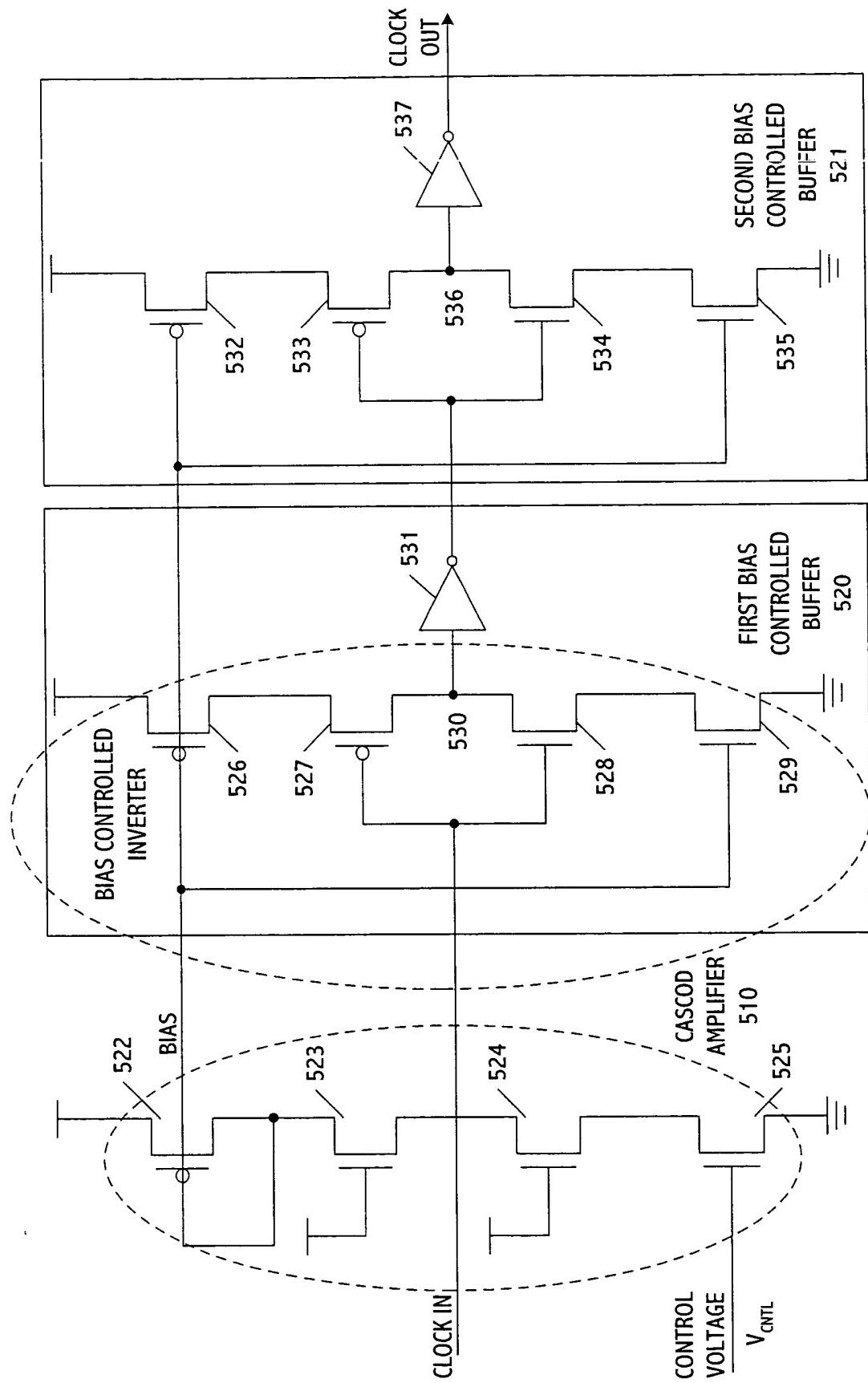


FIG. 5



DUTY CYCLE CORRECTION CIRCUIT PERFORMANCE

INPUT CLOCK DUTY CYCLE

49.20% 49.40% 49.60% 49.80% 50.00% 50.20% 50.40% 50.60% 50.80% 51.00%
40.00% 42.00% 44.00% 46.00% 48.00% 50.00% 52.00% 54.00% 56.00% 58.00% 60.00%

VCB OUTPUT CLOCK DUTY CYCLE
v.s. INPUT CLOCK DUTY CYCLE, FCLOCK - 2GHz

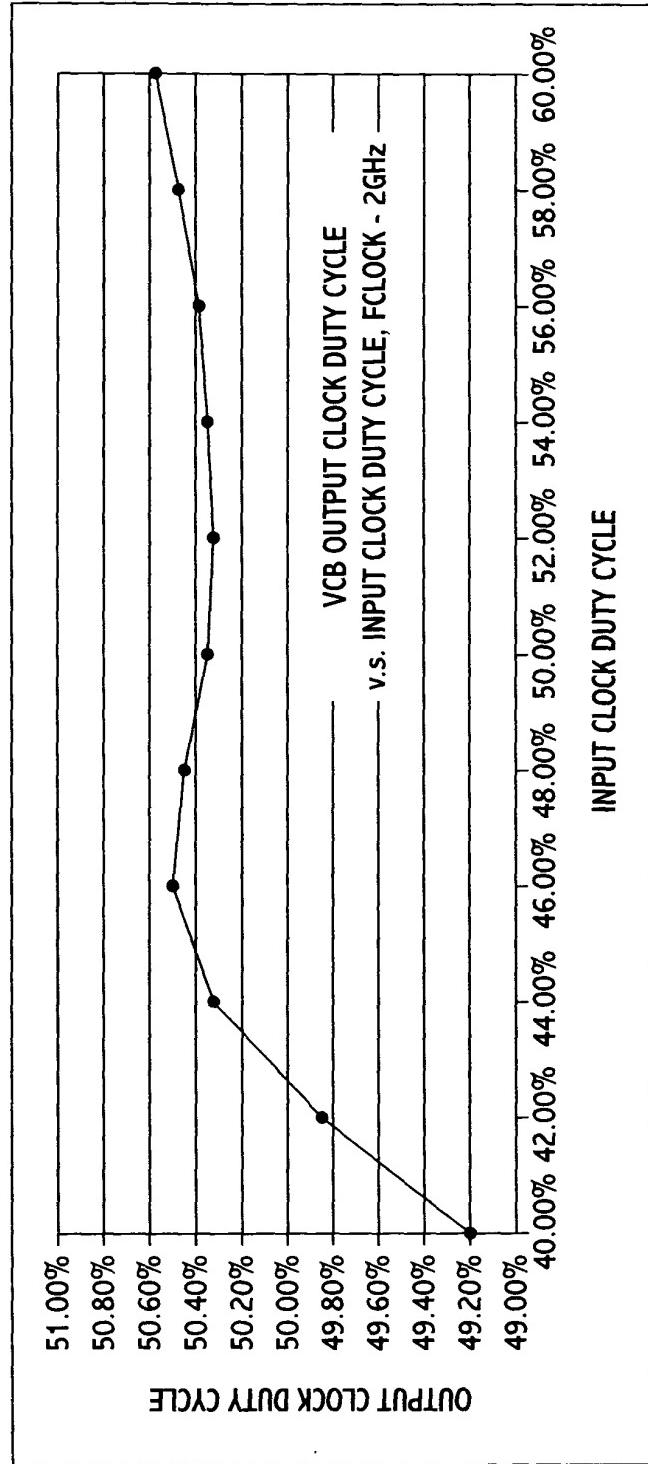


FIG. 6

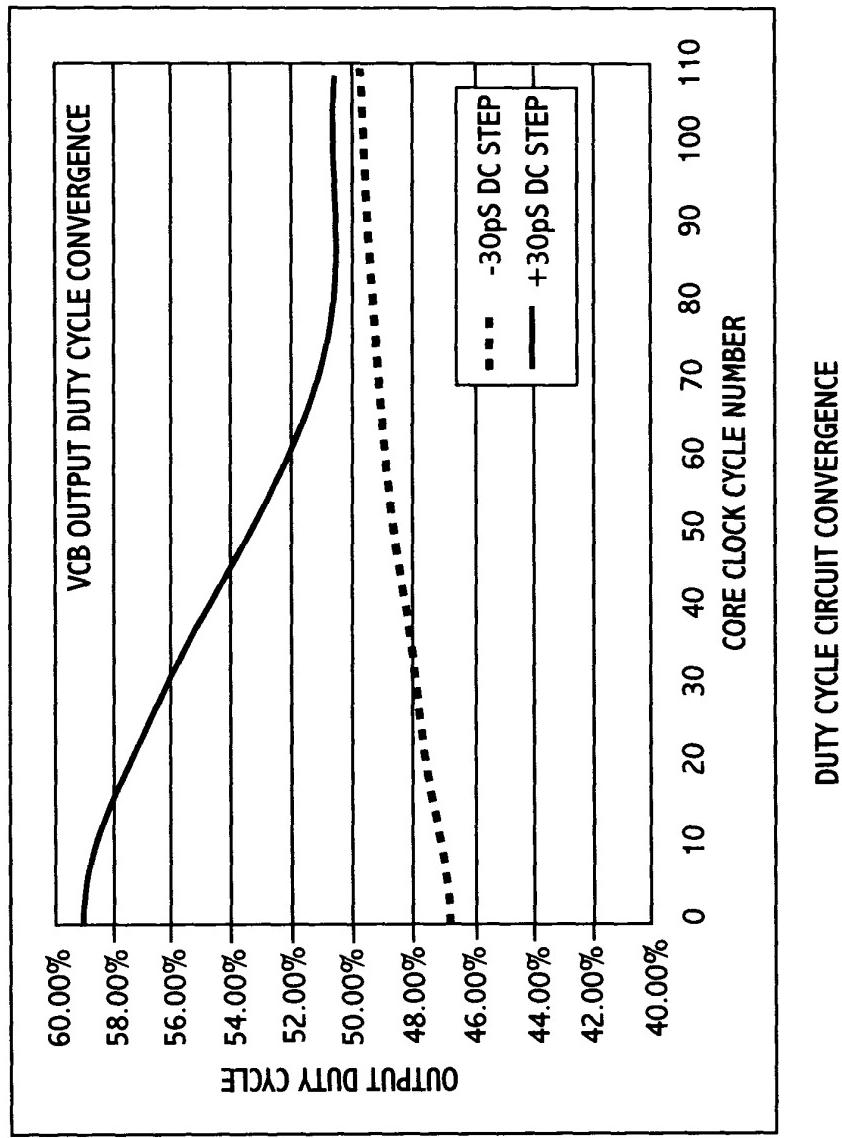


FIG. 7

FIG. 8

